Amendments to the Specification

Please replace the paragraph beginning on page 4, line 28 with the following amended paragraph:

In order to introduce the ions in the SOI layer 13, the impurity concentration of the SOI layer 13 at the FD-MOSFET Df satisfies ~~is satisfied~~ the following ~~formula~~ formulas.

$Df \leq 9.29 * 10^{15} * (62.46 - ts)$ (1)

$Df \leq 2.64 * 10^{15} * (128.35 - ts)$ (2)

Please replace the paragraph beginning on page 5, line 13 with the following amended paragraph:

In order to introduce the ion in the SOI layer 13, the impurity concentration of the SOI layer 13 at the PD-MOSFET Dp satisfies ~~is satisfied~~ the following ~~formula~~ formulas.

$Dp \geq 9.29 * 10^{15} * (62.46 - ts)$ (3)

$Dp \geq 2.64 * 10^{15} * (129.78 - ts)$ (4)

Please replace the paragraph beginning on page 5, line 18 with the following amended paragraph:

Since the impurity concentration of the SOI layer 13 satisfies the formula (3), an N-type MOSFET formed in the SOI layer 13 operates as the partially-depleted MOSFET. Since the impurity concentration of the SOI layer 13 satisfies the formula

(4), and when a drain voltage Vd is 1.5 V and a gate voltage Vg is 0 V, a standby current Ioff that flows from a drain to a source is $2.00 * 10^{-12}$ A/μm or less. That is, since the formula (2) is satisfied, a variation of a gate threshold voltage Vt at the PD-MOSFET ~~FD-MOSFET~~ forming area [[1]] 2 is decreased. The standby current Ioff is defined by a current per a width of a channel region.

Please delete the paragraph beginning on page 5, line 27.

Please replace the paragraph beginning on page 6, line 1 with the following amended paragraph:

As shown in Fig. 3, a field oxide layer 15 is formed between the FD-MOSFET forming area 1 and the PD-MOSFET forming area 2 by a LOCOS process. Then, the N-type MOSFET 20 is formed in the FD-MOSFET forming area 1 and the N-type MOSFET 30 is formed in the PD-MOSFET forming area respectively. The FD-MOSFET 20 includes a gate oxide layer 21, a gate electrode 22 formed on the gate oxide layer 21, a source region 23 having the N-type conductivity, a ~~source~~ drain region 24 with the N-type conductivity and a sidewall structure 26 formed on the gate electrode 22. The PD-MOSFET 30 includes a gate oxide layer 31, a gate electrode 32 formed on the gate oxide layer 31, a source region 33 with the N-type conductivity, a ~~source~~ drain region 34 with the N-type conductivity and a sidewall structure 36 formed on the gate electrode 32. A channel region 25 of the FD-MOSFET 20 is defined between the

source region 23 and the drain region 24. A channel region 35 of the PD-MOSFET 30 is defined between the source region [[24]] 33 and the drain region 34 [[24]]. The source regions 23, 33 and the drain regions 24, 34 are formed by introducing N-type ions.

Please replace the paragraph beginning on page 6, line 17 with the following amended paragraph:

In the present invention, both of the FD-MOSFET 20 and the PD-MOSFET 30 can be formed in the common SOI layer 13 [[with]] while decreasing a variation of an electric characteristic of the MOSFET 20 and 30 ~~is decreased~~.

Please replace the paragraph beginning on page 6, line 20 with the following amended paragraph:

The impurity concentration Df of the SOI layer 13 at the FD-MOSFET forming area 1 can ~~be satisfied~~ satisfy the following formula.

$Df \leq 3.00 * 10^{15} * (102.67 - ts)$ (5)

Please replace the paragraph beginning on page 7, line 3 with the following amended paragraph:

Otherwise, the impurity concentration Dp of the SOI layer 13 at the PD-MOSFET forming area 2 can ~~be satisfied~~ satisfy the following formula.

$Dp \geq 3.29 * 10^{15} * (125.70 - ts)$ (6)

Please replace the paragraph beginning on page 8, line 19 with the following amended paragraph:

When the impurity concentration Df ~~is satisfied~~ satisfies the following formula, the MOSFET is operated as an FD-MOSFET.

$Df \leq 9.29 * 10^{15} * (62.46 - ts)$ (1)

Please replace the paragraph beginning on page 8, line 22 with the following amended paragraph:

When the impurity concentration Dp ~~is satisfied~~ satisfies the following formula, the MOSFET is operated as a PD-MOSFET.

$Dp \geq 9.29 * 10^{15} * (62.46 - ts)$ (3)

Please replace the paragraph beginning on page 12, line 2 with the following amended paragraph:

When the impurity concentration Df of the SOI layer 13 ~~is satisfied~~ satisfies a

following formula (5), the standby current Ioff is $2.00 * 10^{-11}$ A/μm or more. Therefore, the variation σ of the gate threshold voltage Vt of the FD-MOSFET is decreased.

$Df \leq 3.00 * 10^{15} * (102.67 - ts)$ (5)

Please replace the paragraph beginning on page 12, line 18 with the following amended paragraph:

When the impurity concentration Df of the SOI layer 13 ~~is satisfied~~ satisfies a following formula (6), the standby current Ioff is $2.00 * 10^{-13}$ A/μm or less. Therefore, the variation σ of the gate threshold voltage Vt of the PD-MOSFET is decreased.

$Df \leq 3.29 * 10^{15} * (125.70 - ts)$ (5)